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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,240	HOU ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-11 and 13-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-11 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/23/2006.

2. Claims 1-5, 8-11, and 13-19 are pending in this application. Claims 1, 9, 14, and 19 are independent claims. In Amendment, claims 6-7 and 12 are cancelled. This Office Action is made final.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-5, 8-11, and 13-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-5, 8-11, and 13-19 cite a method and system for performing temporal order independent numerical computations according to a mathematical algorithm. In order to claims to be statutory, claims must either include a practical application at useful end or a discrete, useful, and tangible result. However, claims merely disclose a step of manipulate data for numerical computations without including a practical application at useful end or a tangible result(s). The input is a set of number and the output is just another set of number. Therefore, claims 1-5, 8-11, and 13-19 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 14-15 and 18-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Shyu (U.S. 5,471,412).

Re claim 14, Shyu discloses in Figures 4 and 7 a method for performing temporal order independent computations (e.g. abstract and col. 2 line 30 to col. 4 line 56) comprising: receiving a data value for processing (e.g. input into the 4-port data unit 74); determining whether the data value corresponds to one of an addition operation and a multiplication operation (e.g. from the output port of either 735 or 722 and col. 6 lines 32-43); if the data value corresponds to a multiplication operation, storing the data value in a multiplication buffer that stores only data values to which a first mathematical operation performed thereto is multiplication (e.g. col. 7 line 40 to col. 8 line 36, particularly lines col. 7 lines 49-58 wherein the data stored in writeport 1 is transferred to readport 1 to the multiplication computation block 3); if the data value corresponds to an addition operation, storing the data value in an addition buffer that stores only data values to which a first mathematical operation performed thereto is addition (e.g. col. 7 line 40 to col. 8 line 36, particularly lines col. 7 lines 64-68 wherein the data stored in writeport 2 is transferred to readport 1 to the addition/subtraction computation block 2); and outputting a data value stored in the multiplication buffer and an associated data value

stored in the addition buffer to a computation block (e.g. 83 according to the control unit 9) for processing wherein the determining is performed upstream of the computation block.

Re claim 15, Shyu further discloses in Figures 4 and 7 storing partial results generated by the computation block in a TRAM (e.g. 83).

Re claim 18, Shyu further discloses in Figures 4 and 7 the determining step includes determining whether a first mathematical operation to be performed on the data value after being transferred to the computation block is one of the addition operation and the multiplication operation (e.g. col. 3 lines 13-33 and col. 6 lines 45-52).

Re claim 19, it is a system claim of claim 14. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 8-11, 13, and 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Shyu (U.S. 5,471,412).

Re claim 1, Shyu discloses in Figures 4 and 7 a system for performing temporal order independent numerical computations on data (e.g. abstract) comprising: a computation block (e.g. parts 2 and 3 in Figure 4 which computing either multiplication

or butterfly as addition/subtraction as seen in Figure 2A); a buffer block (e.g. 74 in Figure 7), wherein the buffer block (e.g. col. 6 lines 32-42 and the operation of 4-port data unit in Figure 4 is exactly the same configuration for Figure 7) includes at least one first buffer for storing only data values to which a first mathematical operation to be performed thereto after being transferred to the computation block is an addition operation by the computation block (e.g. RP1 as readport for addition/subtraction butterfly operation in Figure 4), and at least one second buffer for storing only data values to which a first mathematical operation to be performed thereto after being transferred to the computation block is a multiplication operation by the computation block (e.g. RP2 as readport for multiplication butterfly operation in Figure 4); and the demultiplexer transmits only to the at least one first buffer the data values to which the first mathematical operation to be performed thereto after being transferred to the computation block is the addition operation by the computation block (e.g. col. 7 line 40 to col. 8 line 36, particularly lines col. 7 lines 64-68 wherein the data stored in writeport 2 is transferred to readport 1 to the addition/subtraction computation block 2), the demultiplexer transmits only to the at least one second buffer the data values to which the first mathematical operation to be performed thereto after being transferred to the computation block is the multiplication operation by the computation block (e.g. col. 7 line 40 to col. 8 line 36, particularly lines col. 7 lines 49-58 wherein the data stored in writeport 1 is transferred to readport 1 to the multiplication computation block 3), and upon a condition, data values are transferred from the buffer block to the computation block for processing (e.g. col. 6 lines 45-53 and by the controller 9 in Figure 7). Shyu

fails to disclose a demultiplexer located upstream from the buffer block. However in the same Figures 4 and 7, Shyu discloses a demultiplexer (e.g. part 1 in Figure 4 or part 71 in Figure 7) for separating the input data to either the multiplication block (e.g. part 3 of Figure 4) or the addition/subtraction block (e.g. part 2 of Figure 4) because it can provide data to either the multiplication or additional/subtraction whenever needed (e.g. col. 5 lines 32-38). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a demultiplexer as seen in Figures 4 or 7 placed in front of the buffer block (e.g. 74) because it would enable to send the provided data to either computation block efficiently (e.g. col. 5 lines 32-38).

Re claim 2, Shyu further discloses in Figures 4 and 7 the first and second buffers are FIFO ("First In First Out") buffers (e.g. inherently from col. 8 lines 36-38 wherein the data is readout sequentially).

Re claim 3, Shyu further discloses in Figures 4 and 7 the computation block computes an IDCT ("Inverse Discrete Cosine Transform") (e.g. col. 8 lines 50-55).

Re claim 4, Shyu further discloses in Figures 4 and 7 eight first buffers are utilized, each corresponding to a column of an 8x8 block of data (e.g. col. 7 lines 40-45).

Re claim 5, Shyu further discloses in Figures 4 and 7 the IDCT is a 2-D IDCT (e.g. col. 9 lines 49-62).

Re claim 8, Shyu further discloses in Figures 4 and 7 the computation block (e.g. 823 and 812 in Figure 9) generates a new partial result utilizing data values transferred from the buffer block (e.g. 74) and the partial result transferred from the TRAM (e.g. 83), the new partial result being then stored back in the TRAM (e.g. 83).

Re claim 9, it has same limitations cited in claim 1. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 1. In addition, Shyu further discloses in Figures 4 and 7 a TRAM block (e.g. 83), wherein the TRAM block stores partial results of the computation between clock cycles (e.g. Figure 8); wherein, upon an occurrence of a predetermined condition (e.g. by the control unit 9 in Figure 7), data values are transferred from the buffer block and the TRAM block to the computation block for processing (e.g. col. 3 lines 1-68).

Re claim 10, it has same limitations cited in claim 3. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 11, it has same limitations cited in claim 4. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it has same limitations cited in claim 5. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 16, Shyu further discloses in Figures 4 and 7 the demultiplexer determines whether the first mathematical operation to be performed on each of the data values after being transferred to the computation block is one of the addition operation and the multiplication operation (e.g. col. 3 lines 15-33).

Re claim 17, it has same limitations cited in claim 16. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Response to Arguments

9. Applicant's arguments filed 08/23/2006 have been fully considered but they are not persuasive.

a. The applicant argues in pages 10-11 for claims 1-5, 8-11, and 13-19 that claims are directed to statutory subject matter because the claims limited to a machine or manufacture which has a practical application in the technologies arts and the claims also define the structure to prevent them from being directed merely to an "abstract idea".

The examiner respectfully submits that, as required by 35 U.S.C. 101, the practical application producing a concrete, useful, and tangible result must exist in the claims instead of the specification and also regardless whether they're implemented in hardware or software. Therefore, claims 1-5, 8-11, and 13-19 are directed to non-statutory subject matter because they fail to disclose the real world application for used the tangible result. Storing the results or the intermediated results would not constitute the practical application.

b. The applicant argues in pages 11-12 for claims rejected under U.S.C. 102 that the cited reference by Shyu fails to disclose the "determining whether the data value corresponds to one of addition operation and a multiplication operation" act and also fails to disclose structurally the determining is performed upstream of the computation block. In addition, the applicant alleges that the cited reference fails to disclose "outputting a data value stored in the multiplication buffer and an associated data value stored in the addition buffer to a computation block" because they can only output one value at a time.

The examiner respectfully submits that the determining act is done or performed by the control unit (e.g. col. 2 lines 46 to col. 3 line 55) wherein the addition operation is done in the butterfly operation 22 and the multiplication operation is done in multiplication operation 33 as seen in Figure 4. In addition, the cited reference clearly discloses the control unit operates to output both data stored in the multiplication buffer (e.g. as the output of second-stage) and the associated data value in the addition buffer (e.g. as the output of first-stage) to a computation block (e.g. the butterfly unit) as seen in column 3 lines 16-22). Thus, the recited reference is clearly capable of outputting both data from the multiplication result and addition result to the computation block for further processing.

c. The applicant argues in page 13 for claims rejected under U.S.C. 103(a) that the cited reference fails to provide a suggestion or motivation to modify as proposed.

The examiner respectfully submits that the motivation or suggestion is clearly stated in the previous Office action for modifying the current prior art as proposed wherein demultiplexer is used to separate or deselect from an input to different outputs. The cited reference clearly discloses functionality of the demultiplexer as to separate or route the appropriated data to either the multiplication block or butterfly block as needed under the command of the control unit. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a demultiplexer in front of the buffer for selectively storing appropriated output result into correct portion of buffer so they can send

out to either multiplier or butterfly unit (e.g. through RP2 or RP1) efficiently. It is efficient because it's reducing inter-wiring within the buffer for reading the data within the 4-port data register unit. With the demultiplexer added in front of 4-port data register unit for routing the stored data to correct place to store, the read-out would be simple by just popping the data in a FIFO manner corresponding to its portion of buffer.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

October 24, 2006

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100